REMARKS

Claims 1, 3 to 5, 7 to 11, 13, 14, 16, 18, 19, and 21 to 34 were pending in the above-identified application when last examined. Applicant has amended claims 9, 13, 18, 19, 21, 29, canceled claims 1, 3 to 5, 7, 8, 10, 11, 14, 26 to 28, and 30 to 34, and added claims 35 to 61. Claims 9, 13, 16, 18, 19, 21 to 25, 29, and 35 to 61 remain pending.

Overview of the Claimed Invention

The claimed invention is directed to a node controller of a node that is distinct from a computer-memory complex of the node. The node controller is coupled to a cluster memory and to a high speed link to another node in a data storage system. The node controller is further coupled by an input/output bus to the computer-memory complex and at least one of a host device and a storage device.

The node controller is the component of the node responsible for data transfer to and from the link. In contrast, the computer-memory complex is responsible for functions related to the control of the node. This split construction has the advantage that the computer-memory complex does not need to be burdened with data transfers and can perform its control functions independent of the data transfer load of the node. This is because the host or storage device may read and write the cluster memory so that the system memory of the computer-memory complex is not burdened with temporarily storing the data being transferred through the node. In addition, the node controller moves the data to another node through the link so that the input/output bus is not burdened with data transfer between nodes. Furthermore, the node controller includes a logic engine can be programmed to write RAID stripes and reconstructs lost data from RAID stripes so that the processor of the computer-memory complex is not burdened with the RAID operations.

Telephone Interview

Applicant thanks the Examiner for the telephone interview on September 12, 2006.

§ 112 Rejections

The Examiner rejected claims 1, 3 to 5, 7 to 11, 13, 14, 16, 28, 33, and 34 under 35 U.S.C. § 112, first paragraph. Specifically, the Examiner did not find support for the claim language of "the

nodes being locally coupled to a same host device and a same data storage device" in the independent claims.

Applicant has canceled claim 1, 3 to 5, 7, 8, 10, 11, 14, 28, 33, and 34, thereby rendering their rejections moot. To expedite prosecution, Applicant has canceled the claim language in question from claim 9. Applicant has amended claims 13 and 16 to depend from claim 18, thereby rendering their rejections moot.

Applicant notes that support for the claim language in question is found in U.S. Application Serial No. 09/633,088, which was incorporated by reference in the Specification. For example, Fig. 7 in U.S. App. Serial No. 09/633,088 illustrates a common host 12 and a common storage device 20 coupled locally to two nodes.

§ 103 Rejections

The Examiner rejected claims 1, 3 to 5, 7, 9 to 11, 13, 16, 18, 19, and 24 to 34 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,642,478 ("Chen et al.") in view of U.S. Patent No. 6,067,063 ("Carpenter et al."). The Examiner rejected claims 8, 14, and 21 to 23 as being unpatentable over Chen et al. and Carpenter et al. and further in view of what is well known in the art.

Canceled claims

To expedite prosecution, Applicant has canceled claims 1, 3 to 5, 7, 8, 10, 11, 14, 26 to 28, and 30 to 34, thereby rendering their rejections moot.

Claims 18

Addressing claim 18, the Examiner cited Chen et al. to disclose all the elements but for both a cluster memory and a system memory. The Examiner then cited Carpenter et al. to show a computer-memory complex with a separate memory for a processor.

Applicant has amended claim 18, which now recites:

> 18. A node controller for a node in a data storage system having at least two nodes, each node comprising one computer-memory complex and one node controller distinct from said one computer-memory complex, the node controller comprising:

a memory controller operable to interface the node controller with (1) a cluster memory that stores data being transferred through the node, and (2) a link coupled to another node controller in another node of the data storage system;

an input/output bus interface operable to interface the node controller with an input/output bus coupled to a computer-memory complex of the node and at least one of a host device and a storage device;

a logic engine coupled to (1) the memory controller, (2) the link, and (3) the input/output bus interface;

wherein in a first type of data transfer, the logic engine performs a logic operation to a plurality of data from one of a plurality of data sources in the data storage system and writes the result of the logic operation to one of a plurality of data destinations in the data storage system, the data sources comprising the cluster memory and the input/output bus interface, the data destinations comprising the cluster memory, the link, and the input/output bus interface, the logic operation being used to calculate a parity data for writing a full or a partial RAID stripe and to reconstruct a lost data using the parity data.

Amended claim 18 (emphasis added).

The combination of Chen et al. and Carpenter et al. does not disclose all the elements of amended claim 18. Carpenter et al. does not show a separate memory for a node processor. Instead, Carpenter et al. shows a system memory 18 that is shared between CPUs 12a to 12d and a node controller 20. The Examiner appears to have cited level 2 (L2) caches 14a to 14d as memories for CPUs 12a to 12d, and system memory 18 as a memory for node controller 20. However, L2 caches 14a to 14d only store frequently accessed data in system memory 18 and therefore they do not form a separate memory that stores different data than system memory 18. Thus, Carpenter et al. does not show separate memories for a CPU and a node processor. Chen et al. does not cure the deficiencies of Carpenter et al.

Furthermore, Chen et al. does not disclose a logic engine that performs a logic operation to calculate parity data for writing a RAID stripe and to reconstruct a lost data using the parity data. While Chen et al. discloses an ECC and memory access protocol logic 52, it does not disclose that ECC and memory protocol logic 52 performs the above described RAID related operations. In addition, Chen et al. does not disclose a node controller with an input/output (I/O) bus interface that couples the node controller with an I/O bus, which in turn is coupled to a computer-memory complex of the first node and at least one of a host device and a data storage device. Carpenter et al. does not cure the deficiencies of Chen et al.

There is no motivation to combine Chen et al. and Carpenter et al. The Examiner stated that "it would have been obvious to one of ordinary skill in the art [to] include a separate memory for the processor, as disclosed by Carpenter, in the system of Chen since this would allow the node processor of Chen its own working memory and closer to the processor as well to increase the memory speed access for the processor." June 19, 2006 Office Action, p. 6. However, Chen et al. does not disclose that node processor 30 requires a local memory or faster memory access. Instead, the Examiner appears to have provided this generic motivation in hind site to justify the combination of Chen et al. and Carpenter et al.

For the above reasons, amended claim 18 is patentable over the cited references.

Claims 9, 13, 16, 19, and 21 to 25

Claims 9, 13, 16, 19, and 21 to 25 depend from amended claim 18. Thus, claims 9, 13, 16, 19, and 21 to 25 are patentable for at least the same reasons as amended claim 18.

Claims 29

Addressing claim 29, the Examiner cited Chen et al. to disclose all the elements but for both a cluster memory and a system memory. The Examiner then cited Carpenter et al. to show a computer-memory complex with a separate memory for a processor.

Applicant has amended claim 29, which now recites:

> 29. A node in a data storage system comprising at least two nodes, the node comprising:
>
> an input/output bus;
>
> a computer-memory complex, comprising:
>
> a central processing unit (CPU);
>
> a system memory storing information for controlling data transfer through the node; and
>
> a controller coupling the CPU, the system memory, and the input/output bus; and
>
> a node controller distinct from the computer-memory complex, the node controller comprising:

a memory controller operable to interface the node controller with a cluster memory of the node, the cluster memory storing data being transferred through the node;

an input/output bus interface operable to interface the node controller with the input/output bus;

a logic engine coupled to the memory controller, the input/output bus interface, and a link to another node of the data storage system;

wherein at least one of a host device and a storage device coupled to the input/output bus is able to read and write the cluster memory via the input/output bus, the logic engine is able to transfer data from the cluster memory to the another node via the link, and the memory controller is able to receive data from the another node via the link.

Amended claim 29 (emphasis added).

The combination of Chen et al. and Carpenter et al. does not disclose all the elements of amended claim 29. As similarly discussed above with regards to amended claim 18, Carpenter et al. does not show a separate memory for a node processor. Instead, Carpenter et al. shows a system memory 18 that is shared between CPUs 12a to 12d and node controller 20. The Examiner appears to have cited L2 caches 14a to 14d as memories for CPUs 12a to 12d, and system memory 18 as a memory for node controller 20. However, L2 caches 14a to 14d store frequently accessed data in system memory 18 and therefore they do not form a separate memory that store different data than system memory 18. In addition, Chen et al. does not disclose a system memory that stores information controlling data transfer through the node and a cluster memory that stores data being transferred through the node. Thus, Carpenter et al. does not show separate memories for a CPU and a node processor. Chen et al. does not cure the deficiencies of Carpenter et al.

Furthermore, Chen et al. does not disclose a node controller with an input/output (I/O) bus interface that couples the node controller with an I/O bus, which in turn is coupled to a computer-memory complex of the first node and at least one of a host device and a data storage device. As such, Chen et al. cannot disclose a host device and a storage device that are able to read or write a cluster memory via the I/O bus. Carpenter et al. does not cure the deficiencies of Chen et al.

As similarly discussed above with regards to amended claim 18, there is no motivation to combine Chen et al. and Carpenter et al. The Examiner stated that "it would have been obvious to one of ordinary skill in the art [to] include a separate memory for the processor, as disclosed by

Carpenter, in the system of Chen since this would allow the node processor of Chen its own working memory and closer to the processor as well to increase the memory speed access for the processor." June 19, 2006 Office Action, p. 8. However, Chen et al. does not disclose that node processor 30 needs a local memory or faster memory access. Instead, the Examiner appears to have provided this generic motivation in hind site to justify the combination of Chen et al. and Carpenter et al.

For the above reasons, amended claim 29 is patentable over the cited references.

New Claims 35 to 61

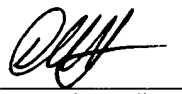
New claims 35 to 47 depend from amended claim 29 and are patentable over the cited references for at least the same reasons as amended claim 29.

New claim 48 to 61 corresponds to pending claims before the European Patent Office. Claim 48 recites similar limitations as amended claims 18 and 29 and is patentable for at least similar reasons as amended claims 18 and 29. New claims 49 to 61 depend from new claim 48 and are patentable over the cited references for at least the same reasons as new claim 48.

Summary

Claims 1, 3 to 5, 7 to 11, 13, 14, 16, 18, 19, and 21 to 34 were pending in the above-identified application when last examined. Applicant has amended claims 9, 13, 18, 19, 21, 29, canceled claims 1, 3 to 5, 7, 8, 10, 11, 14, 26 to 28, and 30 to 34, and added claims 35 to 61. For the above reasons, Applicant respectfully requests the Examiner with withdraw the claim objections and rejections and allow claims 9, 13, 16, 18, 19, 21 to 25, 29, and 35 to 61. Should the Examiner have any questions, please call the undersigned at (408) 382-0480x206.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the date shown below.



Attorney for Applicant(s)

10/2/06

Date

Respectfully submitted,

David C. Hsia
Attorney for Applicant(s)
Reg. No. 46,235